CENTRAL PROCESSOR INSTRUCTION FORMAT

MACHINE CODE

IST.	2nd.	3rd.	4th.	5th.
CHARACTE	CHARACTER	Character	Character	Character
Operation Code	Most Significant Row	Most Significant Column	Least Significant Row	Least Significant Column

OPERATION

M AOORESS (OPERAND)

MODULE ADDRESSING:

For Central Processor Instructions the Module Designation of the Operand is determined by the "X" Bits of the 4th. and 5th. Characters. The following table of bits illustrates Bank Addressing.

"X" BIT Char. 4	"X" BIT Char. 5	MOOULE Oesignation
ABSENT	ABSENT	1
PRESENT	ABSENT	2
ABSENT	PRESENT	3
PRESENT	PRESENT	4

EXTERNAL FUNCTION INSTRUCTION FORMAT

MACHINE CODE

1st.	2nd.	3rd.	4th.	5th.
Character	CHARACTER	Character	CHARACTER	CHARACTER
Function	Sub	Sub	Sub	Sub
	Function	Function	Fuction	Function
	A	B	C	D

1005 80-COLUMN COOE

80-Col. Card Code	Printable Characters	XS-3 Code	80-Col. Card Code	Printable Characters	XS-3 Code
12-1	A	01 0100	7	7	00 1010
12-2	B	01 0101	8	8	00 1011
12-3	C	01 0110	9	9	00 1100
12-4	D	01 0111	12	&	01 0000
12-5	E	01 1000	11	– (minus)	00 0010
12-6	F	01 1001	12-0	?	01 0011
12-7	G H I	01 1010	11-0	! (exclom.)	10 0011
12-8		01 1011	0-1	/	11 0100
12-9		01 1100	2-8	+	11 0011
11-1	J	10 0100	3 – 8	#	01 1101
11-2	K	10 0101	4 – 8	@	10 1110
11-3	L	10 0110	5 – 8	:(colon)	01 0001
11-4	× × × 0	10 0111	6-8	>	11 1110
11-5		10 1000	7-8	'(apos.)	10 0000
11-6		10 1001	12-3 - 8	.(period)	01 0010
11-7 11-8 11-9	P Q R	10 1010 10 1011 10 1100	12-4-8 12-5-8 12-6-8	[11 1101 00 1111 01 1110
0-2	S	11 0101	12-7-8	\$	01 1111
0-3	T	11 0110	11-3-8		10 0010
0-4	U	11 0111	11-4-8		10 0001
0-5	V	11 1000	11-5-8	;(semi-col)	00 0001
0-6	W	11 1001	11-6-8		00 1110
0-7	X	11 1010	11-7-8		10 1111
0 - 8	Y	11 1011	0-2-8	≠	11 0000
0 - 9	Z	11 1100	0-3-8	,(commo)	11 0010
0	0	00 0011	0-4-8	%	11 0001
1	1	00 0100	0 - 5 -8	()	10 1101
2	2	00 0101	0 - 6 -8		00 1101
3	3	00 0110	0 - 7 -8		11 1111
4 5 6	4 5 6	00 0111 00 1000 00 1001	Blonk	Spoce N.P.	00 0000

MEMORY MATRIX

ROW AND COLUMN MACHINE CODE

1	2	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Sp	ľ]	g	4	ř	1	F		1	5	:		2	7	В	8	D	Г	<	#	H	С	1	G	Α	6	?	3	9	E	&	100
1	,	•	1	M	9	Z	₩	,	1	N	80	\$	K	P	S	Q	U	Δ	>	ц	Y	Т	(Χ	/	0	+	L	R	٧	¥)

X ABSENT

X PRESENT



UNIVAC° 1005

EXTENDED SYSTEM

CODE

CENTRAL PROCESSOR INSTRUCTION REPERTOIRE

	SAAL	OPER	DESCRIPTION		CH DE	OPERATION
	LAr	M,L	Load Ascending AR1 or 2	Sp	,	(Mem)(AR1 o) 2)
	LDr	M,L	Load Descending AR1 or 2	1	*	(Mem)-+(AR1 or 2)
	LPR	M,L	Load Print Descending	ø		(Mem)→(Print Buffer)
	SAr	M,L	Store Ascending AR1 or 2	4	М	(AR1 or 2)-+(Mem)
H	SOr	M,L	Store Descending ARI or 2	;	@	(AR1 or2)-+ (Men)
TRANSFER	SPR	M,L	Store Print Descending	1		(Print Bulfer)—(Mem)
=	SHR	M,L S	Shift Right	F		(Mem) - (Mem Ascending)
	SHL	M,L S	Shift Left		_	(Mem)→ (Mem Descending)
	CLR	M,L	Clear Area to Spaces	1		Spaces (Mem)
	SC	M,L C	Store Character		<i>≠</i>	C→ (Mem)
	GAr	M,L	Compare Afpha AR1 or 2	5	N	(ARL or 2): (Mem) Alpha Numeric
A.	CNr	M,L	Compare Numeric ARI or 2	:	%	(AR1 or 2): (Mem) Algebraic
COMPARE	IC	M	Inciement and Compare	_		(Mem) Update(Mem)
ŏ	CCA	M,L C	Compare Character Alpha		#	(Mem); C Alpha Numeric
	J	M	Jump Unconditional	2		(Branch-+(Mem)
	Je	M	Jump Greater (Numeric)	В		(Branch (Mem) if Greater
	JL	R	Jump Less Than (Numeric)	7		(Branch- (Mem) if Less
	JL	M	Jump Equal (Numeric)	7		(Branch→ (Mem) : [Equal
	JEA	M	Jump Equal (Alpha Numeric)	3	-	(Branch - (Mem) if Equal
ü	JUA	M	Jump Unequal (Alpha Numeric)	,	\vdash	(Branch(Mem) if Unequal
JUMP LOGIC	JP	M	Jump Positive (Arithmetic)	7		(Branch (Mem) if Positive
A N	JN	M	Jump Negative (Arithmetic)	8		(Branch-+(Mem) If Negative
7	JZ	M	Jump Zero (IC & Arithmetic)	8		(Branch—(Mem) of Zero
	JR		Store PAK in X REG - Jump	1		(PAK)→(X REG), (Branch→(Mem)
	JX	M	Store X REG in M	Γ		(X REG)→(Mem)
	JS3	M	Jump Att Switch 3	Ė	٧	(Branch-+(Mem) # Alternate Switch 3 on
	JOF	M	Jump Arithmetic Overflow	\vdash	٧	(Branch(Mem) if Arithmetic Overflow
	AMr	M,L	Add Alg ARI or 2 to M	<	>	(ARI or 2) + (Mem)-(Mem) w Sign Compare
	JOF	M,L	Add Aig. M to AR1 or 2	#	п	(Mem)+(AR) or 2)-+(AR) or 2) w Sign Compare
ETIC	SMr	M,L	Subtract Alg. AR1 or 2 from M	Н	γ	(Mem) - (AR1 or Z) → (Mem) w Sign Compare
ARITHMETIC	SRr	M,L	Subtract Alg M from ARI or 2	С	Т	(ARI or 2)-(Mem)-(ARI or 2) w Sign Compare
Æ	MUL	M,L	Multrply	<		(Mem) x (AR1)(AR2)
	DIA	M,L	Divide	G		(AR2 ÷ (Mem) → (AR1 and 2)
	TRL	M,L	Translate	<		(Mem)(Mem) Translated
	SZS	M,L	0 Supress AR2 & Stole Ascending		9	(ARZ Edited)→(Mem)
	LWS	M,L	Load AR2 w/Sign & Zone Delete	-	?	(Mem) (AR2 with Edit)
=	LMr	M,L	Zone Defele AR1 or 2	3	L	(Mem)→(ARI or 2 w Zone Delete)
EDI	SED	M,L	Edif AR2 & Store Ascending		R	(AR2 Edited)→(Mem)
	LAH	M,L C	Logical And	<u> </u>	#	(M) ∧ C → (M)
	LOH	M,L C	Fosical Or		#	(M) ∨ C → (M)
	BSH	M.L	Bit Shift Circularty		≠	Shift (1 Chi Mem) Cucularly One Bit

INPUT/OUTPUT - INSTRUCTION REPERTOIRE

1	SAAL	OPER	DESCRIPTION	MACH CODE	OPERATION
J	PTE		Punch Test	E	(Processor Interlock) If Punch Active
	XF	REA	Read Card	8	Caid→(Caid Buffer)
	XF	PR1	Print – SP1	8	(Print Buffer) Printer SP1
	XF	PR2	Print - SP2	å	(Print Bulfer) Printer SP2
	χF	PR7	Print - SK7	8	(Print Buffer) - Printer - Channel 7 Dn Loop
	XF	PUN	Punch	8	(Punch Buffer)→ Punch
	ΧF	RPR	Read ~ Print -SP1	8	Caid→(Caid Buffer) (Print Buffer)→ Printer — SP1
	XF	RP2	Read - Print - SP2	8	Card - (Card Bulfer) (Print Buffer) - Printer - \$P2
	XF	RPH	Read - Punch	8	Card → (Card Buffer) (Punch Butter) → Punch
	XF	RPP	Read - Pi+nt - SP1 - Punch	8.	Uard → (Card Butter) (Print Butter) → Printer - SP! (Punch Butter) → Punch
Æ	XF	SH2	Skip 2	8.	(Advance Paper)→ Channel 2 On Loop
SYSTEM	XF	SX4	Skip 4	8	(Advance Paper) Channel 4 Dn Loop
	ΧF	SX7	Skip 7	8	(Advance Paper)— Channel 7 On Loop
CARD	XF	RCI	Read Code Image	8	Caid→(Buffer Code Image)
-	XF	PCI	Punch Code Image	8	(Punch Buffer Code Image)→ Punch
	XF	RXC	Read Auxiliary Code Image	8	Card Aux Reader → (Buffer Code fmage)
	XF	RX1	Read Auxiliary Sikr Sel 1	8	Card Aux Reader→ (Buffer) Stkr Sel 1
	χF	RX2	Read Auxiliary Stkr Sel 2	ā	Card Aux Reader→ (Buffer) Slkr Sel 2
	XF	RRS	Read Auxifiary Stkr Sel 3	#	Card Aux Reader—(Buffer) 5thr Sel 3
	XF	PSS	Punch Stkr Sel	å	(Punch Buffer)→ Punch Stkr Sel
	XF	RRP	Read Read Punch	*	Card Punch (Read/Punch input Buffer) (Read Punch
	ΧF	RRS	Read/Read Punch Stkr Sel	8	Outpuf Buffer) — Punch Card Punch — (Read/Punch Input Buffer) (Read Punch
N.	XF	RRC	Read/Read Punch Code Image		Output Buffer) Punch Stki Sel Card Punch (Read/Punch Input Butter Code Image)
	XFC	MACHINE	Special Instructions	8	(Read Punch Output Buffer Code Image)→ Punch Input Output Card System Combinations
-	XF	RP1	Read Paper Tape I Frame	8	Paper Tape—(Buffer) 1 Frame
	XF	RPS	Read Paper Tape 80 Frames	å	Paper Tape → (Buffer) 80 Frames
	XF	RPS	Read Paper Tape Through Sentinel	4	Paper Tape→(Buffer) Through Sentine!
E E	XF	PP1	Punch Paper Tape 1 Frame	#	(Punch Buffer 1 Frame) - Paper Tape Punch (No Parity)
TAPE	XF	PPS	Punch Paper Tape to Sentinel	4	(Punch Buffer To Sentinel) Paper Tape Punch (No Parity)
٦	XF	PIP	Punch Paper Tape 1 Frame	#	(Punch Buffer Frame) - Paper Tape Punch (w/Parity)
d	XF	PSP	Punch Paper Tape to Sentine	<i>*</i>	(Punch Buffer To Sentinel) - Paper Tape Punch (w/Parity)
U	JPE	M	Jump Parety Error	V	Branch-(Mem) If Parity Error
n	JCS	M	Jump Channel &	v	Branch (Mem) If Channel 8
-	XF	RT _s ,BF _n ,L	Read Tape Normal Gain	* *	Mag Tape-(Buffer) Normal Gain
	XF	RTs+4,BFn,L	Read Tape High Gain	<i>≠</i>	Mag Tape-(Buffer) High Gain
2	XF	WTs,BFn,L	Write Tape	<i>≠</i>	(Buffer) Mag Tape
C TAPE	XF	ERs.BFn.L	Erase Before Write	±	Erase Mag Tape — (Bulfer) — Mag Tape
Ē	XF	1	Backspace 1 Block	<u></u>	Backspace
MAGNETIC	XF	BS _E	Reward Servo	<u></u>	Rewind
Z	-	HW ₈	Jump Parity Erroi	\	Branch→(Mem) ff Parity Error
	JPE	M	Jump End of Tape	T v	Branch→(Mem) # End of Tape
٣	-		-	v	
14 ×	XF	SHB	Send DLT 80 Characters Send DLT Through Sentinel	V V	(Buffer)—I DLT 80 Characters
W	XF	SHS		l v	(OLT) Buffer
DATA LINE TERMINAL 3	XF	RCO	Receive DLT to EDM	V	Bianch (Mem) If Pairty Ellor
I N	JPE	M	Jump Parity Eleor	+	Branch (Mem) IT Parity Error Branch (Mem) End of Time (No Traffic 20 Seconds)
M	JET	M	Jump End of Time	٧	
à	PTE	AL F- (Pause Test DLT	E	(Processor Interlock) If DLT Active
	XF	SI ₁ ,BF _n ,L	Send Buffer to 1001	V	L Buffer Characters → 1001 Buffer
00	XF	RI1,BFn,L	Receive from 1001	V	(Oata)—Buffer
٦	JII	M	Jump Interrupt Unit 1	٧	Branch—(Mem) If 1001 Ready
	JAL	M	Jump Alert	V	Branch—(Mem) ff 1001 Interfocked

s = Servo Number

1005 INPUT/OUTPUT-STORAGE AREAS

2		2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	3L	3
1	1	a	•		ı	,	1	•	,	18	п	12	19	14	10	18	11	18	и	20	a	22	10	ы	41	46	11	20	29	11	11	F
2	22	83	64	26	14	87	10	24	49	11	8 2	12	44	45	40	47,	56	41	16	01	11	84	54	89	54	97	10	82		01	94	ŀ
3	93	88	"	99	97	18	**	10	11	12	19	14	14	19	77	н	19	\$6	ex.	82	11	4		н	ŧΪ	=	19	11	91	92		ŀ
4	и	15	н	87	81	19	198	191	102	102	100	185	156	187	400	188	£3:0	m	112	376	114	335	115	m	113	218	128	121	122	141	126	ŀ
5	125	126	337	136	128	139	101	132	111	184	130	134	131	138	100	100	141	100	141	144	163	146	141	144	149	156	151	152	182	156	155	ŀ
6	156	107	158	168	799	191	112	261	184	201	ш	167	194	763	110	171	372	172	170	116	179	111	178	170	156	192	182	183	144	145	186	ŀ
,	187	769	289	156	291	102	192	284	195	111	197	781	199	200	201	282	287	284	295	299	287	198	201	244	211	214	213	414	218	218	217	ŀ
8	218	224	228	221	222	222	724	241	128	221	210	229	288	231	242	224	234	285	200	231	238	229	200	281	242	254	244	245	254	241	249	ł
9	449	219	263	252	643	251	256	158	251	251	218	264	261	262	263	564	264	416	281	410	280	419	271	212	212	274	210	278	217	276	278	ŀ
0	280	283	262	280	216	260	244	287	411	285	256	587	282	229	21/2	20%	298	287	234	Zee	344	201	\$62	\$61	284	385	306	34 7	304	201	719	ŀ
1	922	54]	23.%	314	216	31.5	21.F	Ωŧ	211	326	123	121	323	324	325	\$26	321	32t	329	232	231	121	\$21	341	425	336	3.01	\$28	185	246	145	l
2	347	\$43	384	146	246	341	148	349	250	151	152	250	264	355	254	381	348	331	240	35%	382	253	\$E1	368	368	36)	366	359	378	130	372	İ
3	873	974	979	279	872	878	979	160	\$81	992	989	284	161	\$49	387	549	389	201	411	114	111	894	211	441	197	449	399	148	411	141	161	١
4	884	40 5	405	487	491	409	613	411	413	613	014	415	626	427	110	435	429	421	422	423	424	625	425	621	428	429	420	431	432	123	634	İ
5	165	436	427	616	435	441	627	437	443	443	437	436	441	446	427	456	145	462	453	456	145	165	105	105	416	162	461	145	436	562	445	t
6	887	109	655	469	786	786	786	786	786	186	786	786	116	786	un	811	519	519	684	103	186	786	109	469	451	781	402	105	449	449	199	İ
7	497	683	169	510	519	811	519	669	109	534	454	500	819	514	489	511	186	116	786	716	186	449	273	519	613	689	689	529	126	526	E27	t
8	128	126	666	540	522	528	934	443	548	362	562	841	562	541	642	562	962	165	546	145	546	196	560	862	145	145	611	881	666	667	666	İ
8	145	685	562	562	562	56 2	562	562	562	562	553	165	145	145	165	145	145	811	887	574	881	588	111	188	188	145	881	881	688	588	***	Ì
0	145	811	E 82	562	887	696	196	681	681	445	\$60	EES	659	545	165	605	685	811	887	987	811	811	811	103	***	887	m	8111	252	***	254	İ
1	887	103	786	189	786	186	116	185	629	858	187	***	***	887	601	151	105	524	685	E48	881	109	140	543	645	887	189	103	624	685	109	I
2	887	811	252	616	156	145	616	859	145	562	887	165	"	887	881	#11	962	605	881	811	***	***	***	165	145	887	811	811	601	811	811	Ī
3	685	109	685	E48	109	786	786	786	105	109	786	109	881	887	881	648	109	140	7116	114	116	786	785	109	181	2116	109	186	111	111	494	I
1	8 87	***	716	127	165	145	720	145	811	811	145	145	811	165	887	E48	E48	681	801	E48	254	661	881	685	738	145	748	145	811	549	548	1
6	145	786	786	E40	***	***	#11		t 11	***	252	811	109	145	1116	109	784	186	186	109	111	186	611	881	811	786	786	111	7116	716	685	I
6	786	316	786	105	E48	786	786	186	116	786	786	386	549	786	250	811	881	811	881	811		***	E48	116	100	801	103	109	786	186	106	I
1	887	786	m	883	189	186	786	116	186	186	786	784	186	186	114	786	103	116	***	926	611	881	540	920	109	784	109	E34	781	685	837	-
6	252	811	841	из	881	151	151	252	111	811	***	111	154	***	881	£11	#11	811	151	***	252	801	881	562	881	811	***	796	786	881	801	
6	881	611	***	***	***	***	811	786	***	811	***	111	811	56 2	811	tii		580	***	181	811	841	811	111		888	•••	***	en	109	109	
0	284	861	941	994	994	194	мі	90	м	138	410	511	924	910	124	916	929	127	979	919	974	121	922	421	924	925	526	921	528	424	934	1
11	981	932	121	929	981	186	997	128	539	116	941	342	144	144	941	441	941	868	142	950	011	914	911	414	955	916	987	101	989	311	982	
2												8	T	AT	ıc	A	EG	118	T	E PI	8											ŀ

MOOULE 2

_				ARI	ITKM	ETIC	REG	137 E F	11											4RIT	HMET	IC R	EGIST	ren 2									
32	ī	2	Ī	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	

MACHINE ADDRESSES:	FROM		TO
MEMORY MODULE 1	0001	_	0961
MEMORY MODULE 2	0962	_	1922
MEMORY MODULE 3	1923		2883
MEMORY MODULE 4	2884	_	3844

r = Register 1 or 2
M = Most Significant Location
L = Length of Operand
C = Character Stored in the Instruction
A = Lopica And in the Instruction
V = Lopicat Or

BFn = Memory Module (1 (hrough 4)

L = Length of Operand